Introduction

Zilker Labs' digital power conversion products use an innovative digital filter in the regulation control loop. This digital filter offers advantages over conventional analog filters in that it more easily compensates the control loop as described in this document.

Background

This document describes the compensation method for a digitally controlled, closed loop, switching power converter technology. In control theory, the control loop is usually broken into two parts: the plant and the compensator. The plant is simply the system without the compensator. The compensator is a specialized circuit that compensates or modifies the response of the system so that the closed loop system is stable in the presence of disturbances.

The Plant

The schematic of a typical synchronously rectified, buck derived, power conversion system is shown in Figure 1. A PWM controller controls the relative 'on' times in a complimentary manner for the high side and low side switches. When on, the high side switch (FET) allows the current to increase in the inductor and when off, the inductor current flows through the low side (FET) and the current decreases during this period. The inductor and capacitor (with their respective parasitic elements, e.g. Rc) form a filter which reduces the switching ripple as seen by the load (Ro) to an acceptable value as determined in the design process.

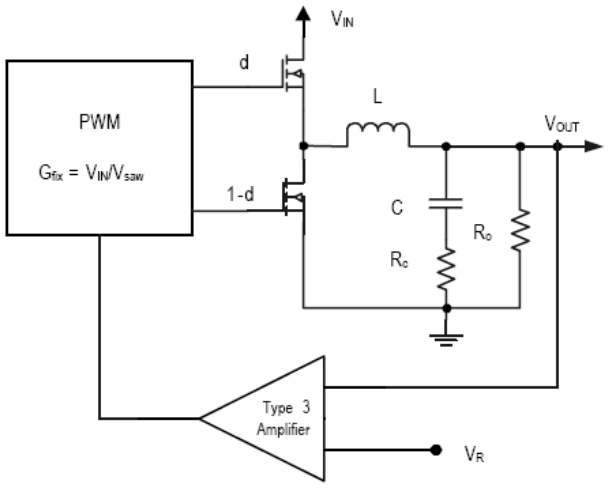

Figure 1. Closed Loop Voltage Regulator System

As can be seen in Figure 1, there is an input to the PWM that controls the duty cycle and there is an output, Vout. The PWM itself introduces a gain called the modulation gain, G_{fix}. A gain function can be written which describes the ratio of the output versus the input to the PWM.

This gain function is:

$$G_P = G_{fix} \frac{1+\frac{s}{\omega_{esr}}}{\frac{s^2}{\omega_n^2}+\frac{s}{Q\omega_n}+1} \quad \text{Eq. 1}$$

where:

ω_{esr} ≡ the frequency of the zero due to the esr of the output capacitor

ω_n ≡ the "natural" frequency of the output stage

Q ≡ the quality factor of the output stage

For the purpose of this application note, the zero due to capacitor esr will be ignored and focus is placed on poles of the remainder of the transfer function. That transfer function is:

$$G_S = G_{fix} \frac{1}{\frac{s^2}{\omega_n^2}+\frac{s}{Q\omega_n}+1} \quad \text{Eq. 2}$$

where:

$$\omega_n = \frac{1}{\sqrt{LC}} \quad \text{Eq. 3}$$

$$Q = Ro\sqrt{\frac{C}{L}} \quad \text{Eq. 4}$$

The equation above has two poles. For Q<0.5 (damped case), both poles are real. For Q>0.5 (underdamped case), the poles are complex conjugates.

Figure 2 shows a plot of this function for several values of Q, a natural frequency of 16kHz and a modulation gain of 5 (14 dB). The top graph shows the magnitude of the gain and the bottom graph shows the phase of the gain function.

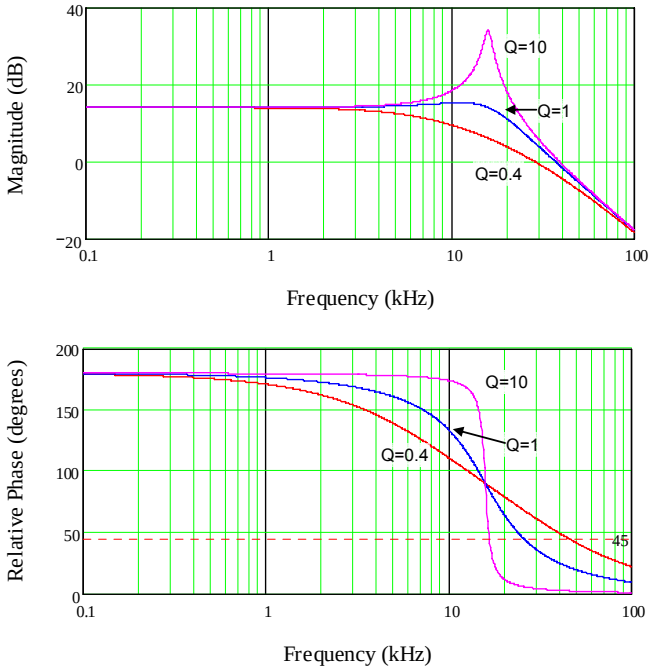

Figure 2. Bode Response of Plant

In terms of robustness with respect to perturbations, the above plant (and typical power conversion plants) has poor performance.

- Since it is desired to regulate the output around its DC set point, a high gain at DC or low frequencies…much more than 14 dB…is preferred, but to add the gain at high frequencies, where noise would be amplified, is not a goal. Typically this is achieved by adding a pole at zero frequency with the compensator. If this is done, the gain of the system for frequencies above the natural frequency falls much too quickly resulting in a system that is unstable. So, along with the pole at zero, a compensator is needed that compensates the poles associated with the natural frequency of the plant.

- To first order, a simple goal would be to cancel the poles with corresponding zeros to give the system a response that looks something like a simple pole at zero frequency.
- The gain crossover frequency (bandwidth) should be adjusted to achieve balanced performance between transient response and sensitivity to noise. If the bandwidth is too low, the system will have inadequate response to transient loads on the output. If the bandwidth is too high, the control system will produce a noisy output.

The Compensator

In Figure 1, the compensator is illustrated as a "Type 3" compensator which is standardized terminology for an analog filter network which provides proportional, integral, and derivative feedback to compensate the system. In the control process, the output voltage is compared to a reference (V_R) to generate an error signal. The error (actually, the negative of the error) is modified by the compensator. The modified error then controls the PWM generator to close the control regulation loop.

As mentioned above, there are three types of modifications that the compensator can perform on the error signal. This three term compensator is abbreviated as PID. "Proportional" (P) refers to a portion of the error that is allowed to pass with only a gain being applied. "Integral" (I) refers to integrating a portion of the error and allowing this integral value to contribute to the modified error signal. Finally, the "derivative" (D) modification refers to allowing the derivative of the error signal to be added to the modified error. The P and I elements insure that the error is driven to zero and the D element reacts to changes in the error.

Zilker Labs products use a digital filter to provide the PID compensation. Digital PID offers more flexibility and better compensation than its analog counterpart. Zilker Labs tools have fields for G, F and Q (gain, frequency, and Q) coefficients to provide an intuitive and easy method for compensation input. Although direct access to the respective gains for each of the three PID taps is available, it is convenient to use these analog coefficients.

Given G, F, and Q, compensation is now simply a matter of aligning the natural frequency of the compensator to the natural frequency of the plant, then adjusting the Q of the compensator to the Q of the plant, and finally adjusting the gain, G, to achieve the desired bandwidth for stable operation.

Stability Goals

The system will be unstable if the phase is 180 degrees when the magnitude of the gain is 1 (0dB). How close the transfer function approaches this condition characterizes the stability of the system. Stability is characterized in terms of phase margin and gain margin. Phase margin is defined at the crossover frequency (gain of 1 or 0 dB) as the amount of phase difference from 180 degrees of phase. Gain margin is defined as the difference from unity gain when the phase is 180 degrees.

Typically, good margin is defined by a phase margin of 45 degrees or greater and a gain margin of 6 dB or more.

Compensation

Compensation is typically done in several stages depending on the amount of information available about the plant at each stage of the design process. The basic steps in compensation are the same no matter the amount of information about the plant.

Steps:

1. Determine the natural frequency of the plant. (Eq. 3)
2. Determine the Q of the plant. (Eq.4)
3. Use the derived values of F and Q from steps 1 and 2 for the respective compensator settings.
4. Adjust the compensator G to give the desired stability and transient response.
5. Optional: Adjust Q and G within the limits of the stability goals to optimize transient performance.

Zilker Labs provides a tool, CompZL, to facilitate the initial compensation of the controller design. The tool allows the model of the plant to be entered. The relevant equations are handled by the tool.

Figure 3 shows a bode plot generated by the CompZL tool. The peak on the right is due to the plant response and the dip to the left is the anti-resonant response of the compensator.

Visually, you can quickly determine the natural frequency of the plant (step 1) and the Q (step 2). These values are then entered into the tool to align the compensator to the plant (step 3). Finally, the gain, G, can be adjusted to give the desire stability margins.

Use of the CompZL tool facilitates the initial design. Final design should be validated on actual hardware using a network analyzer using the same procedure.

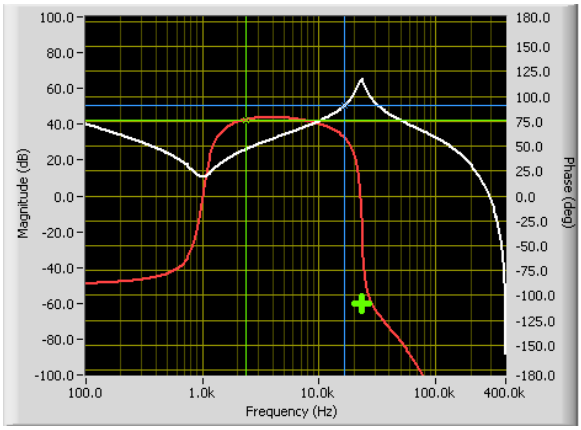

Figure 3. CompZL Bode Simulation

Introduction to CompZL

CompZL is a powerful, easy-to-use software tool that enables optimization of Proportional - Integral - Derivative (PID) compensation parameters for any of Zilker Labs' Digital-DC™ power conversion products for a specific power stage schematic design. Automatic optimization mode predicts the optimal PID settings based on real-world performance criteria, and manual optimization mode enables the user to adjust the compensation performance based on actual laboratory measurements using an intuitive process.

This application note will discuss the methodology for obtaining the required PID settings using automatic optimization mode and manual mode and will offer an example scenario for comparison.

User Console

The CompZL tool is based on a simple yet powerful user console (see Figure 4). This console allows the designer to accurately model their power stage schematic and enter desired performance criteria relative to loop compensation as well as to view the predicted results graphically and with specific output data.

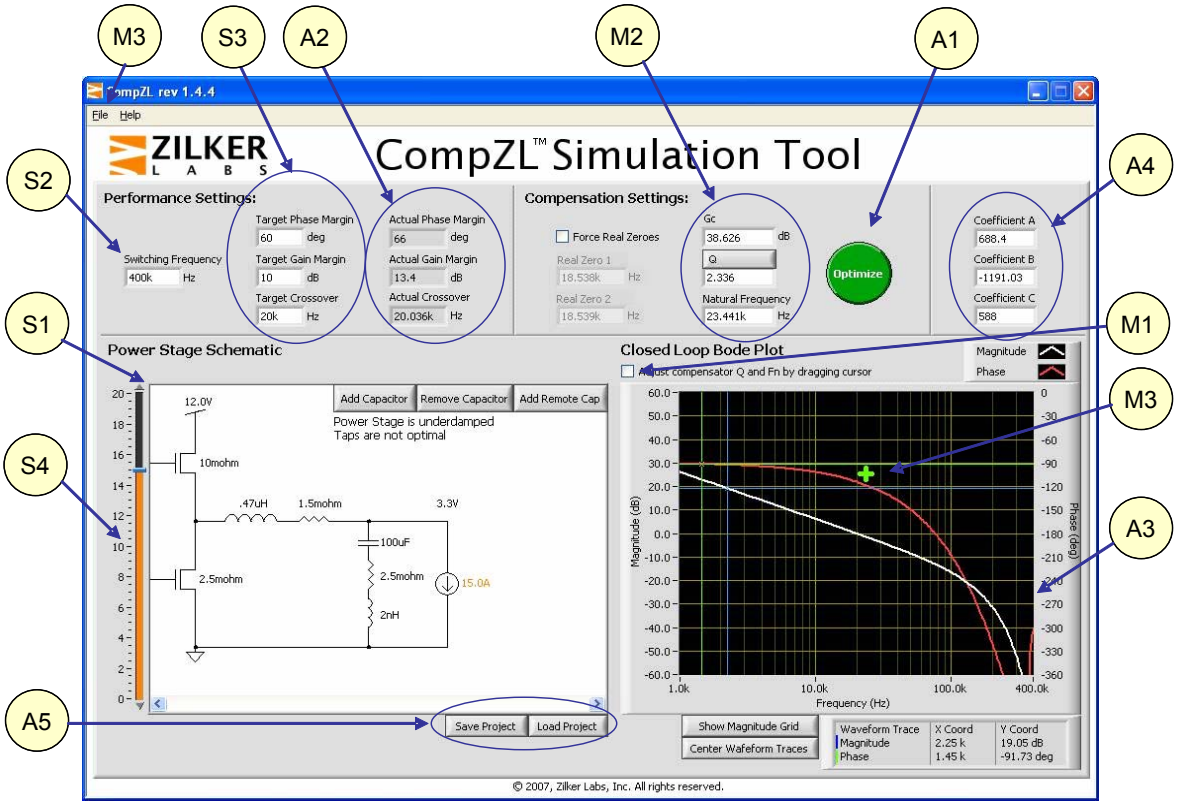

Figure 4. CompZL User Console

Power Stage Model Setup

In order to predict the correct compensation settings, the power stage schematic must first be configured to include models of the components used in the converter circuit.

Upon start-up, CompZL will include a sample schematic from which the actual schematic model can be derived. This initial schematic includes a pair of synchronous MOSFETs, an output inductor, and an output capacitor. The parasitic resistance element of the inductor and inductive/resistive elements of the capacitors are also included for accuracy.

The value of any component may be modified by either double-clicking on the component (including the input voltage source and load) and entering the desired value in the pop-up window or by clicking once on the component and using the slider bar (S4) to adjust the component value.

The following steps may be followed to configure the power stage schematic:

Set the input source. Use the slider bar (S4) or double-click the input source to select the appropriate input voltage if different from the default.

Double-click the upper MOSFET and enter the equivalent R_{DSON} value of the MOSFETs selected for the actual circuit. Repeat for the lower MOSFET.

Double-click the output inductor and enter the value of the inductance to match the selected component's inductance at the selected load current and switching frequency. Best results are generally achieved using the average of the minimum and nominal inductance values. Double-click the inductor resistive element and adjust the value to match the ESR of the inductor at the selected load current and switching frequency.

Double-click the output capacitor and adjust its capacitance value to match the value of the actual capacitor selected. Double-click the inductive and resistive elements of the capacitor and enter the appropriate values individually. These values should match the parameters provided by the component supplier at the selected switching frequency, DC Bias and temperature.

Click the *Add Capacitor* button to add additional capacitors to the model. Enter the desired values into the pop-up window and then click OK.

Click the *Add External Capacitor* button to add a transmission line model and additional capacitors external to the transmission line. Click OK when done.

System Constraints and Output Results

CompZL will accept several system constraints as the basis for calculation of the PID compensation settings.

- Switching Frequency in Hz (S2)
- Desired phase margin in Degrees (S3)
- Desired gain margin in dB (S3)
- Desired crossover frequency in Hz (S3)

Given these system constraints, the optimization engine will attempt to match the desired phase margin, gain margin, and crossover frequency. The predicted values are displayed individually (A2) and a graphical representation of the closed-loop Bode plot (A3) is created. The corresponding PID compensation values A, B, and C (A4) are also displayed on screen so they can be loaded into the appropriate Digital-DC device.

Additionally, the power stage schematic screen will display text related to the status of the power stage and the status of the PID taps. If any of the input constraints are varied sufficiently to cause a new optimization process, the screen will display the message "Taps are not optimal."

Automatic Optimization Mode

Once the power train schematic model is correctly configured and the input constraints have been entered, clicking the *Optimize* button (A1) will initialize the internal automatic optimization mode. This mode uses an internal optimization routine to produce the best fit of phase margin, gain margin, and crossover frequency for the selected power train and switching frequency. The optimization algorithm adjusts the complex compensation zeroes to produce a phase response that is as flat as possible while achieving the gain required to meet all three conditions.

Once the best fit compensation settings have been calculated, the PID taps will be displayed in green text and the Power Train Schematic screen will reflect optimal tap settings. The PID compensation values (A4) will be presented in red text if they have not yet been optimized; once the optimization routine has been run they will be displayed in green text. The *Actual Crossover* frequency field will also be displayed in green text.

It should be noted that the automatic optimization mode will attempt to optimize the compensator response based on the power stage circuit model entered by the user. Components often change their characteristic behavior as the switching frequency is varied; accordingly, the parasitic characteristics of each device should be modified when the switching frequency is modified. Most component data sheets provide the device characteristics versus frequency. It is also possible to measure the component characteristics using a precision impedance analyzer.

Manual Optimization Mode

The CompZL tool offers several methods of manually adjusting the compensation settings to optimize the circuit response.

Manual Cursor Adjust Mode

If a slightly different response characteristic is desired after using the automatic optimization mode, it is possible to *adjust* the compensator zeros by moving the cursor on the Bode plot manually until the desired response is observed graphically. Clicking the check box (M1) just above the Bode plot enables this mode. Dragging the cursor (M3) enables changes in Q and crossover frequency but does not adjust the gain of the compensator. Gain adjustments can be made

by entering a new value in the Gc field (M2).

Manual Parametric Entry Mode

Manual parametric entry mode can be used to tweak the compensator response slightly from the output of automatic optimization mode or to manually adjust the compensator gain, damping, and frequency response based on actual Bode plot measurements of the circuit.

This mode utilizes values entered into the input fields (M2) for Gain (Gc), Q (damping), and natural frequency to modify the compensator response in an intuitive manner such that the user can quickly determine the optimal compensation values to achieve the desired Bode plot response.

Saving Your Work

It is possible to save the circuit configuration and resultant compensation settings to a file for later review. Clicking the *Save* button (A5) will open a new window prompting the user to save the file in .CZL format. Select a name and an appropriate location for this file. The file may also be saved by clicking the File menu (M3) and selecting *Save Project* from the drop-down menu.

Loading Previously Saved Files

Any file that has been saved in the .CZL format can also be loaded into CompZL at a later time by clicking the *Load* button (A5) or by clicking the *File* menu (M3) and selecting *Load Project* from the drop-down menu.

Exporting PID Taps

Once the PID compensation settings have been calculated, they may be saved to a file for loading into the appropriate Digital-DC devices. Click the *File* menu (M4), select *Export PID Taps* from the drop-down menu, and input the desired file name and location for the file. This file is saved in .TXT format and can be loaded into a Digital-DC device using the PowerNavigator™ Evaluation Software.

Design Example

This section walks the designer through a typical design procedure using CompZL. Refer also to AN2011 (Component Selection Guide), AN2016 (Digital-DC Control Loop Compensation), AN2039 (Second Order Effects to Compensation of DDC Products) and AN2032 (NLR Configuration of DDC Products).

The following design constraints are given:

- Input Voltage: V_{IN} = *12 V ± 2 V*
- Output Voltage: V_{OUT} = *1.5 V ± 5 %*
- Maximum Output Current:
  I_{Omax} = *30 A*
- Inductor Ripple Current: ΔI_L = *30%·I_{Omax} = 9 A*
- Switching Frequency: f_{sw} = *300 kHz*
- Output Voltage Ripple:
  $\Delta V_{Ostatic}$ = *±1%·V_{OUT} = ±15 mV*
- Output Voltage Transient Response, pk-pk:
  $\Delta V_{Otran-pp}$ = *±5%·$V_{OUT-nom}$ = ±75mV*
  ΔI_{Otran} = *50%-100%-50% = 15 A*
  dI_O/dt = *2.5 A/µs*
- Target Phase Margin:
  PM_{min} = *53°*
- Target Gain Margin:
  GM_{min} = *6 dB*
- Target Crossover Frequency:
  f_{xo} = *15kHz*
- Target Efficiency:
  $\eta \geq 88\%$ *@ 50%·I_{Omax}*
  $\eta \geq 85\%$, *15%·$I_{Omax} \leq I_O \leq I_{Omax}$*
- Ambient and PCB Temperatures:
  T_{AMB} = *45 °C*
  T_{PCB} = *65 °C*
- Controller:
  ZL2006

Step 1 – Choose an inductor, considering the effects on inductance of the initial tolerance, DC bias and switching frequency. The maximum current rating of the inductor should also be greater than the maximum output current plus half the ripple current. The minimum desired inductance is given by:

$$L_{\min-des} = \frac{\left(1-\frac{V_{OUT}}{V_{IN\max}}\right)\cdot V_{OUT}}{\Delta I_L \cdot f_{sw}}$$

$$L_{\min-des} = \frac{\left(1-\frac{1.5V}{14V}\right)\cdot 1.5V}{9\,A\cdot 300\,kHz}$$

$$L_{\min-des} = 0.496\mu H$$

The IHLP5050FDERR68M01 seems a good choice.

- Nominal Inductance: L_{nom} = *0.68 µH*
- Inductor Resistance:
  DCR = 1.4 mΩ, *ESR @ 300kHz ≈ 14 mΩ*
- Inductor Current Rating:
  I_{SAT} = *60 A,* I_{THERM} = *35 A*
- Initial Tolerance: δL_{tol} = *20 %*
- DC Bias: δL_{bias} *≈ 10.3 %*
- Frequency: $\delta L_{freq} \approx$ *5 %*
- Root-Sum-of-Squares of all deviations:

$$\delta L_{RSS} = \sqrt{\delta L_{tol}{}^2 + \delta L_{bias}{}^2 + \delta L_{freq}{}^2}$$

$$\delta L_{RSS} = \sqrt{(20\%)^2 + (10.3\%)^2 + (5\%)^2}$$

$$\delta L_{RSS} = 23.05\%$$

- Minimum Probable Inductance:

$$L_{\min} = L_{nom} \cdot (1 - \delta L_{RSS})$$

$$L_{\min} = 0.5233\ \mu H$$

- Maximum Probable Ripple / Peak Currents:

$$\Delta I_{L\max} = \frac{\left(1-\frac{V_{OUT}}{V_{IN\max}}\right)\cdot V_{OUT}}{L_{\min}\cdot f_{sw}}$$

$$\Delta I_{L\max} = \frac{\left(1-\frac{1.5V}{14V}\right)\cdot 1.5V}{0.5233\,\mu H\cdot 300\,kHz}$$

$$\Delta I_{L\max} = 8.531\,A$$

$$\tfrac{1}{2}\Delta I_{L\max} = 4.266\,A$$

$$I_{Lpeak} = I_{O\max} + \tfrac{1}{2}\Delta I_{L\max}$$

$$I_{Lpeak} = 30\,A + 4.266\,A = 34.266\,A$$

- Inductance Value for CompZL:
  L_{calc} = *½ (L_{nom} + L_{min}) = 0.6016 µH*

Step 2 – Choose an output capacitor solution that satisfies the Output Voltage Ripple and Transient specs and that has ripple current capacity greater than the worst-case Inductor Ripple Current. Since the Output Voltage Transient Response was specified as peak-to-peak, first the Output Voltage Ripple budget and the controller's regulation error over line, load and temperature is subtracted to determine our actual budget for the transient response alone.

$$\Delta V_{Otran\text{-}max} = \Delta V_{Otran\text{-}pp} - \Delta V_{Ostatic} - \varepsilon_{reg}$$

$$\Delta V_{Otran\text{-}max} = 5\% - 1\% - 1\% = 3\%$$

AN2011 outlines a method for selecting output capacitors when a single type of output capacitance is used. However, in this example, the designer chooses to absorb some of the inductor ripple current with ceramic capacitors and provide additional bulk capacitance using Aluminum Conductive Polymer technology. The designer selects a *47 µF* ceramic capacitor in a *1206* package and a *6.3 V, 820 µF* Al-Poly capacitor in a *10.3 mm x 10.3 mm x 12.2 mm* SMT can package. From electrical characteristics data obtained from the ceramic capacitor supplier, the designer learns the following parameters and de-ratings:

- Equivalent Series Resistance @ *300 kHz, 85 °C, 1.5* V_{DC}: $ESR_{cer} \approx 1.56\ m\Omega$
- Equivalent Series Inductance: $ESL_{cer} \approx 1.13\ nH$
- Ripple Current Rating for *20 °C* rise: $I_{ac\text{-}cer} \approx 3.2\ A$
- Initial Tolerance: $\delta C_{tol\text{-}cer} = 20\ \%$
- DC Bias of *1.5 V*: $\delta C_{bias\text{-}cer} \approx 10\ \%$
- AC Voltage of *30 mV*: $\delta C_{ac\text{-}cer} \approx 15\ \%$
- Temperature of *65 °C*: $\delta C_{temp\text{-}cer} \approx 20\ \%$
- Root-Sum-of-Squares of all deviations:
  $\delta C_{cer} = \sqrt{\delta C_{tol-cer}{}^2 + \delta C_{bias-cer}{}^2 + \delta C_{ac-cer}{}^2 + \delta C_{temp-cer}{}^2}$
  $\delta C_{cer} = \sqrt{(20\%)^2 + (10\%)^2 + (15\%)^2 + (20\%)^2}$
  $\delta C_{cer} = 33.54\%$
- Minimum Probable Ceramic Capacitance:
  $C_{\min-cer} = C_{nom-cer} \cdot (1 - \delta C_{cer})$
  $C_{\min-cer} = 31.24\,\mu F$

From electrical characteristics data obtained from the Al-Poly capacitor supplier, the designer learns the following parameters and de-ratings:

- Equivalent Series Resistance at *300 kHz*: $ESR_{Al\text{-}Poly} \approx 10\ m\Omega$
- Equivalent Series Inductance at *300 kHz*: $ESL_{Al\text{-}Poly} \approx 5\ nH$
- Ripple Current Rating for *20 °C* rise: $I_{ac\text{-}Al\text{-}Poly} \approx 5.5\ A$
- Initial Tolerance: $\delta C_{tol\text{-}Al\text{-}Poly} = 20\ \%$
- Temperature of *65 °C*: $\delta C_{temp\text{-}Al\text{-}Poly} \approx 15\ \%$
- Root-Sum-of-Squares of all deviations:
  $\delta C_{Al-Poly} = \sqrt{\delta C_{tol-Al-Poly}{}^2 + \delta C_{temp-Al-Poly}{}^2}$
  $\delta C_{Al-Poly} = \sqrt{(20\%)^2 + (15\%)^2}$
  $\delta C_{Al-Poly} = 25.00\%$
- Minimum Probable Al-Poly Capacitance:
  $C_{\min-Al-Poly} = C_{nom-Al-Poly} \cdot (1 - \delta C_{Al-Poly})$
  $C_{\min-Al-Poly} = 615\,\mu F$

For multiple-type output capacitors, the simplest and most accurate way to determine how many of each type of capacitor to use is by simulation. From simulation results, the designer determines to use four ceramics and four Al-Polys to meet ripple and transient specs. This equates to the following:

- Effective Ceramic Capacitance
  $C_{eff\text{-}min\text{-}cer} = 124.96\ \mu F$
  $ESR_{eff\text{-}cer} \approx 0.39\ m\Omega$
  $ESL_{eff\text{-}cer} \approx 0.2825\ nH$
- Effective Al-Poly Capacitance
  $C_{eff\text{-}min\text{-}Al\text{-}Poly} = 2460\ \mu F$
  $ESR_{eff\text{-}Al\text{-}Poly} \approx 2.5\ m\Omega$
  $ESL_{eff\text{-}Al\text{-}Poly} \approx 1.25\ nH$

Step 3 – Select MOSFETs that satisfy efficiency, cost and availability requirements. In this example, the designer selects the Infineon BSC030N03LS (x1 high-side) and BSC016N03LS (x2 low-side).

Typical Drain-Source On-State Resistance,
BSC030N03LS: *3.8 mΩ @ V_{GS} = 4.5V*
BSC016N03LS: *1.8 mΩ @ V_{GS} = 4.5V*

Predicted efficiency is shown in Figure 5.

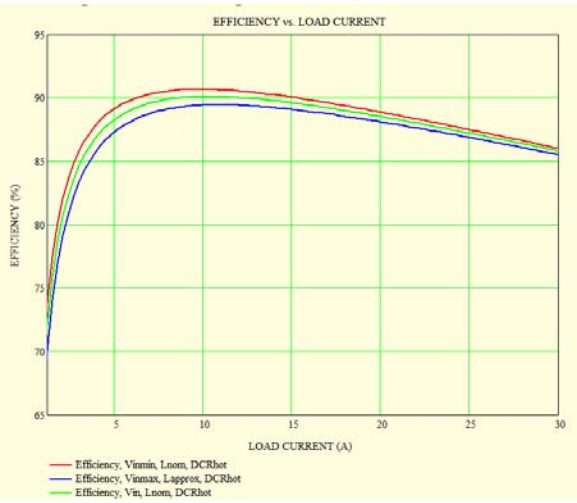

Figure 5. Predicted Efficiency

Step 4 – Enter Component Parameters and Design Constraints into CompZL. It is very important that these entries accurately reflect actual component values under target bias conditions to achieve good correlation between predicted and measured results.

- *Vin = 12V*
- *$R_{DSon-HS}$ = 3.8 mΩ*
- *$R_{DSon-LS}$ = 1.8 mΩ / 2 = 0.9 mΩ*
- *L_{calc} = 0.6016 µH*
- *R_L = 14 mΩ*
- Capacitor Type 1:
  - *C_1 = 31.24 µF*
  - *ESR_{C1} = 1.56 mΩ*
  - *ESL_{C1} = 1.13 nH*
  - *Qty_{C1} = 4*
- Capacitor Type 2:
  - *C_2 = 615 µF*
  - *ESR_{C2} = 10 mΩ*
  - *ESL_{C2} = 5 nH*
  - *Qty_{C2} = 4*
- *Vout = 1.5 V*
- *Iout = ½ΔI_{Lmax} = 4.266 A*
- *f_{sw} = 300 kHz*
- *PM_{min} = 53°*
- *GM_{min} = 6 dB*

Step 5 – Compare Compensation Options and make your selection. Figure 6 and Figure 7 show the expected response of CompZL's optimizer using both the under-damped and over-damped switch settings respectively. The resulting compensation and expected response for each case is a product of performing CompZL's automatic compensation on the components chosen in the previous steps. These results have the advantage of good gain across the response band while still meeting phase margin requirements. The compensation result in Figure 6 yields complex zeroes that more perfectly cancel the complex poles of the output filter itself. However, the real zeroes compensation of Figure 7 results in more mid-band gain which may in practice yield better transient response.

In Figure 8 and Figure 9, the compensator zeroes have been manually adjusted to yield a straight-line magnitude response and flat phase response below crossover at load currents of one-half the inductor ripple current and I_{max}, respectively, with a significant increase in phase margin and a slight reduction in gain margin (relative to Figure 6 and Figure 7). These results might be used in an adaptive compensation scenario.

Figure 10 uses the natural frequency of Figure 6 with a lower Q and compensator gain to yield even more mid-band loop gain without sacrificing bandwidth. This approach generally yields very good transient response across the entire load range.

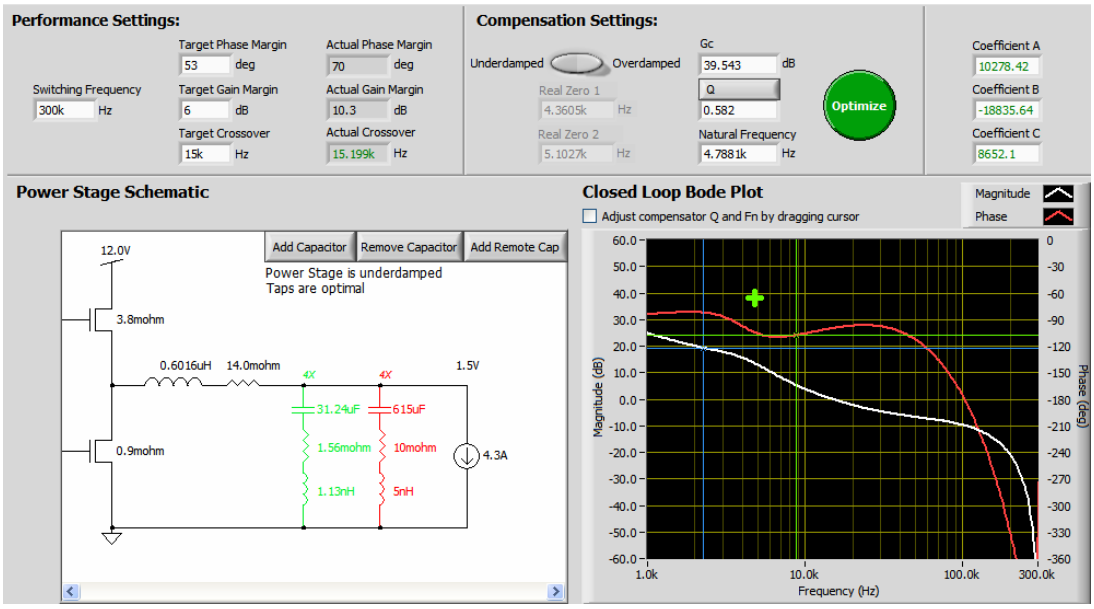

Figure 6. CompZL Under-Damped Optimizer Results

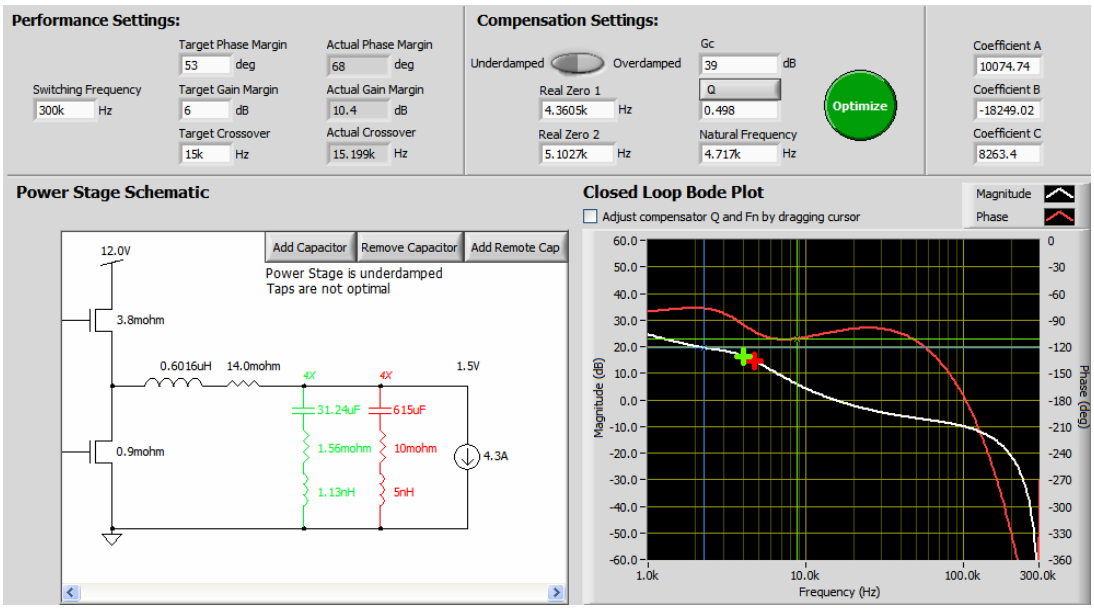

Figure 7. CompZL Over-Damped Optimizer Results

The Next Step – Compensation Verification and Optimization. CompZL uses a simplified model and relies on accurate component parameters provided by the designer to make predictions of system performance. The actual circuit will have higher-order effects, parasitic impedances and complex component behaviors that will cause differences between predicted and measured results that increase with switching frequency. Therefore, CompZL should be used for preliminary selection of compensation settings and the designer should next verify and optimize the compensation according to the procedure outlined in this application note. Finally, the designer should follow the procedure outlined in AN2032 (NLR Configuration of DDC Products) to select NLR settings, if NLR is required for the application.

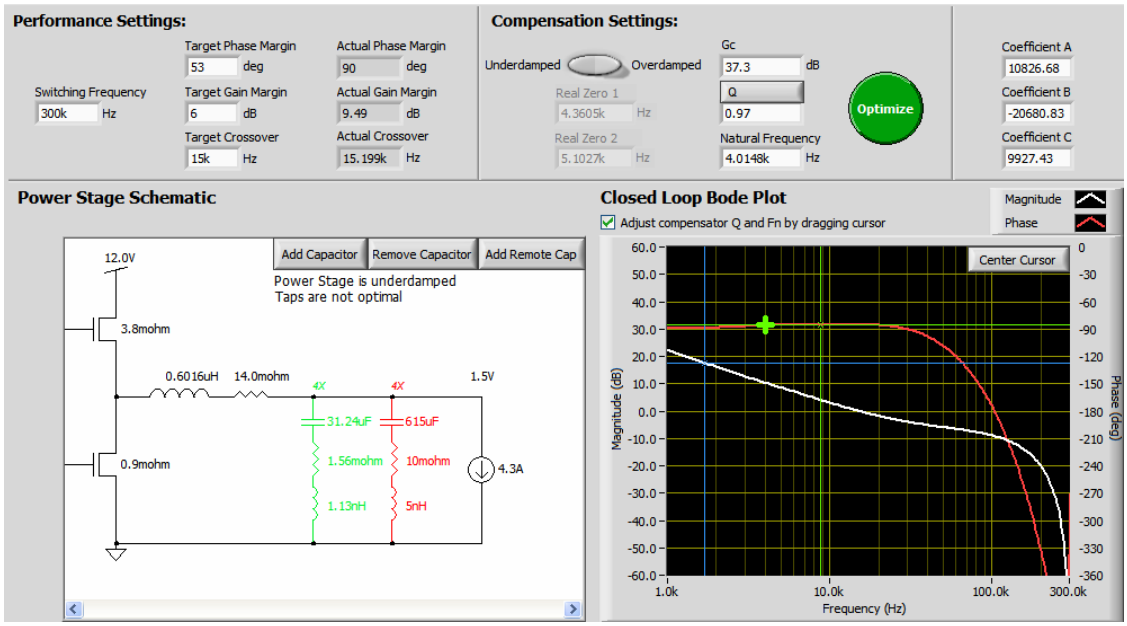

Figure 8. CompZL Manual Results, Straight-Line Magnitude, Flat Phase, $\frac{1}{2}\Delta I_{Lmax}$

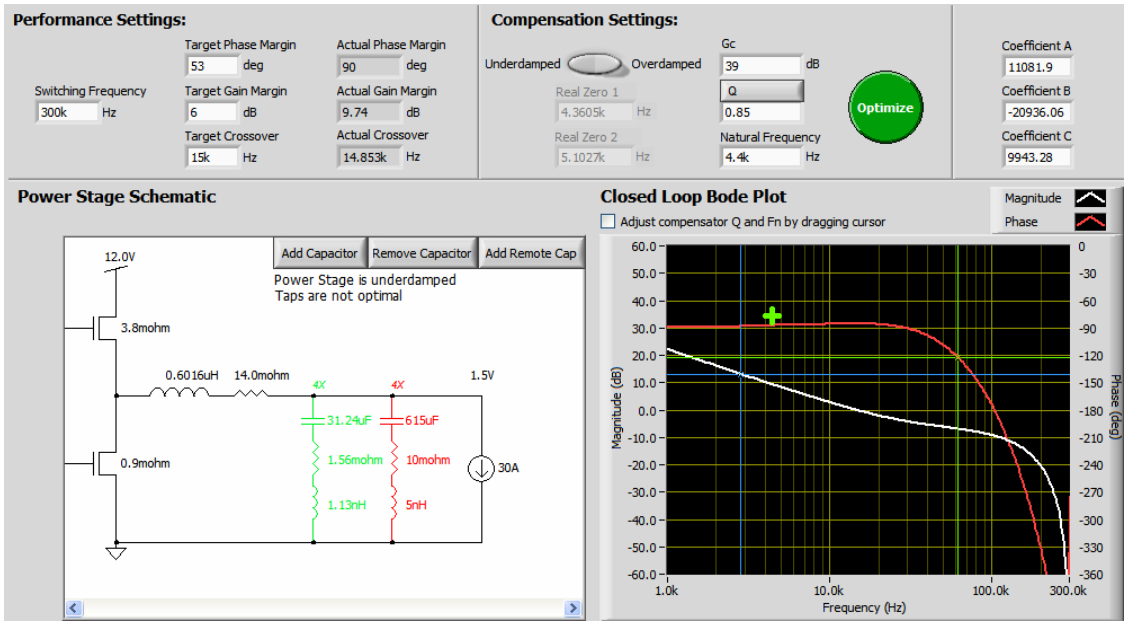

Figure 9. CompZL Manual Results, Straight-Line Magnitude, Flat Phase, I_{max}

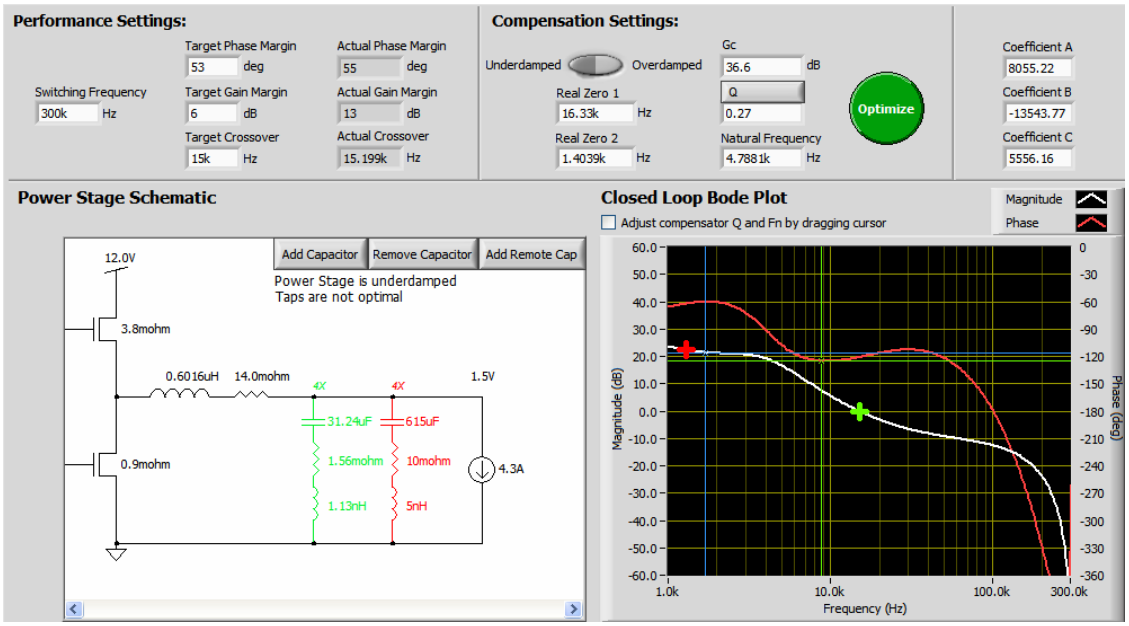

Figure 10. CompZL Manual Results, with Mid-Band Gain Boost

References

[1] AN2011 – *Component Selection Guide*, Zilker Labs, 2007.

[2] AN2016 – *Digital-DC Control Loop Compensation*, Zilker Labs, 2007.

[3] AN2032 – *NLR Configuration of DDC Products*, Zilker Labs, 2008.

[4] AN2039 – *Second Order Affects to Compensation of DDC Products*, Zilker Labs, 2008.

Revision History

Date	Rev. #	
November 2008	1.0	Initial Release
April 2009	0	Assigned file number AN2035 to app note as this will be the first release with an Intersil file number. Replaced header and footer with Intersil header and footer. Updated disclaimer information to read “Intersil and it’s subsidiaries including Zilker Labs, Inc.” No changes to datasheet content.

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